

FIG. 1

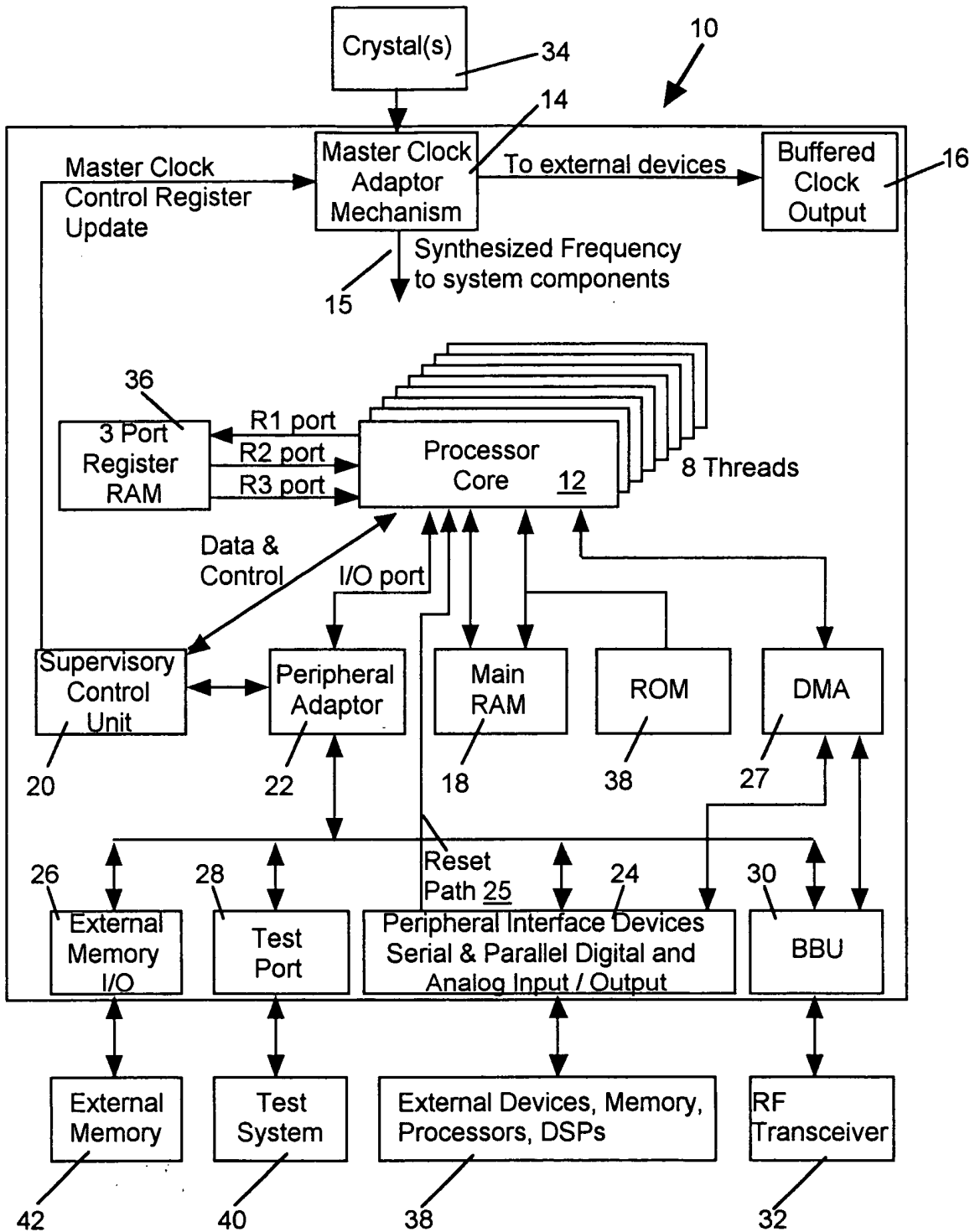


FIG. 2

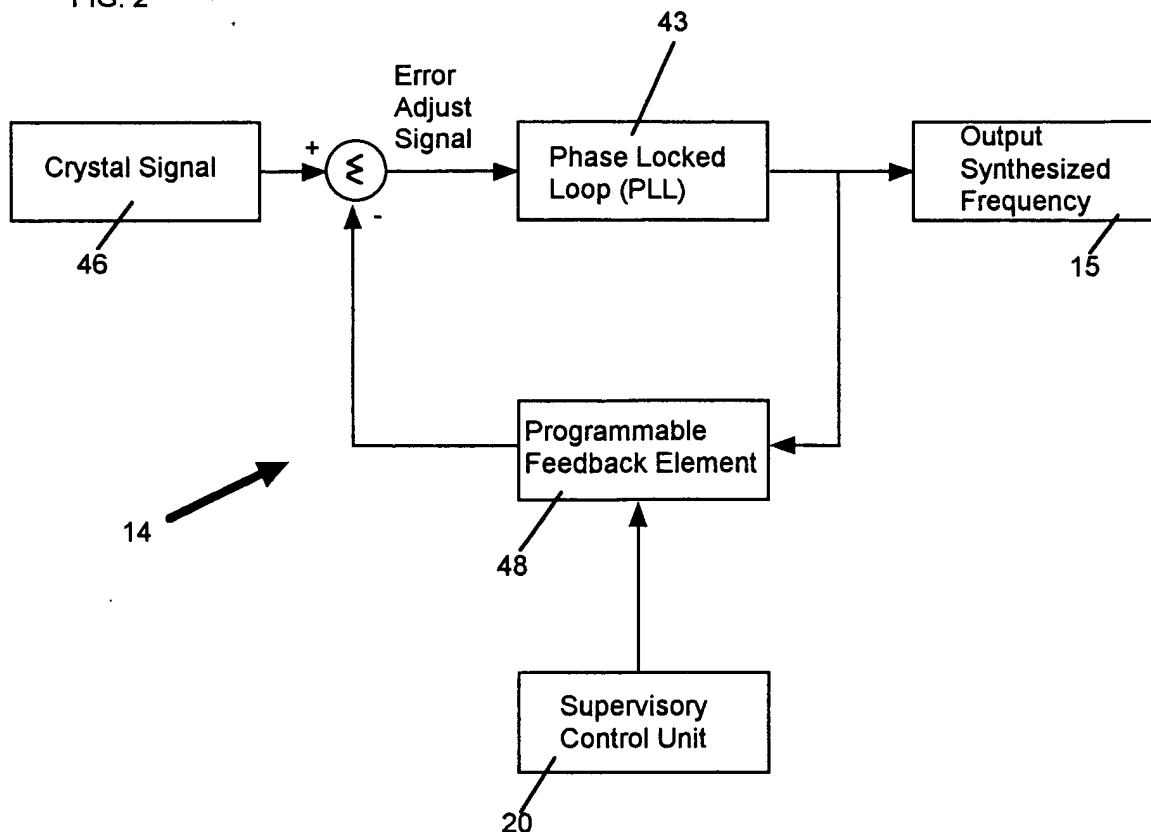


FIG. 3

ADDRESS	READ	WRITE	
0	Register R0...R7	Register R0...R7	138
1	Program Counter	Program Counter	136
2	Condition Code	Condition Code	134
3	Break Point	Stop	132
4	Wait	SCU Access Pointer	112
5	Semaphore Vector	Up Vector	109
6	RESERVED	Down Vector	110
7	Time	Master Clock Control Register	44

118 points to address 0  
120 points to address 1  
122 points to address 2  
124 points to address 3  
126 points to address 4  
128 points to address 5  
130 points to address 7



FIG. 5

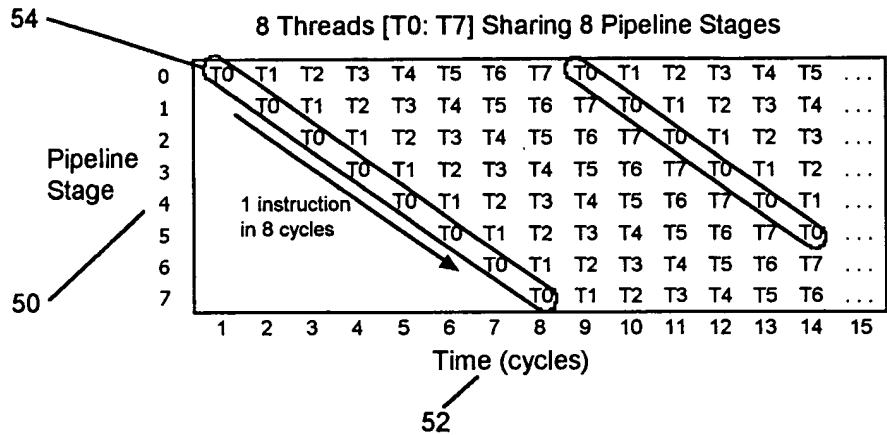


FIG. 6

PIPELINE STAGE Stage # Description		RESOURCE SAGE - Processor Logic or System Memory							
		Instruction Fetch Logic	ROM or 2 Port Main RAM	Instruction Decode Logic	Register RAM (3 port)	Address Mode Logic	ALU	Peripheral Adaptor Logic	Branch /Wait Logic
0	Instruction Fetch	Used	Read						
1	Instruction Decode			Used					
2	Register Reads				Read				
3	Address Modes					Used			
4	ALU Operation						Used		
5	Memory or I/O Cycle		Read or Write					Read or Write	
6	Branch/Wait								Used
7	Register Write				Write				Used

58

56

FIG. 7



FIG. 8

Instr.	Description	Available Address Modes
add	2's complement add	register, immediate
and	bitwise and	register, immediate
bc	conditional branch	PC relative
bic	bit clear	immediate
bis	bit set	immediate
bix	bit change	immediate
bra	unconditional branch	PC relative
inp	read input port	immediate
ior	bitwise inclusive or	register, immediate
jsr	jump to subroutine	register indirect, absolute
ld	load from RAM	base displacement, absolute
mov	move immediate	immediate
outp	write output port	immediate
rol	bitwise rotate left	register, immediate
st	store to RAM	base displacement, absolute
sub	2's complement subtract	register
thrd	get thread number	register
xor	bitwise exclusive or	register, immediate

FIG. 9

Address Mode	Description	1-Word	2-Word
register	Rn	yes	no
register indirect	*Rn	yes	no
base displacement	*(Rn+K)	yes	yes
PC relative	*(PC+K)	yes	yes
absolute	*K	no	yes
immediate	K	some	some